Hall Ticket No: | | | | | | | | | | |

Question Paper Code: 25MBVESTC03

MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(Deemed to be University under Section 3 of UGC Act, 1956)

M.Tech. I Year II Semester (R25) Regular End Semester Examinations - June 2026

CMOS ANALOG IC DESIGN

(VLSI Design and Embedded Systems)

Time: 3Hrs **Max Marks: 100**

All parts of a question must be answered in one place only.
Answer one question from each of Units I to V

Q.No.	Question	Marks	CO	BL
	UNIT-I			
Q.1.	Examine the second-order effects such as channel length modulation and body effect impact circuit performance.	20 M	1	4
	OR			
Q.2.	Illustrate the impact of short channel effects such as DIBL, velocity saturation, punch through, and hot carrier effects on the operation of MOSFET devices.	20 M	1	3
	UNIT-II			
Q.3.	Discuss the working and operation of Gilbert Cell. How is it used as a multiplier in analog signal processing applications?	20 M	2	3
	OR			
Q.4.	Discuss the working principle and operation of Current Mirror with a neat sketch.	20 M	2	2
	UNIT-III			
Q.5.	Derive the expression for the overall time constant of a cascode amplifier.	20 M	3	4
	OR			
Q.6.	Describe the causes and frequency characteristics of thermal noise and flicker noise.	20 M	3	3
	UNIT-IV			
Q.7.	Illustrate the role of gain boosting in operational amplifiers. How does it impact output resistance, gain, and stability?	20 M	4	4
	OR			
Q.8.	Analyse how the addition of a second stage in an op amp affects gain and output swing.	20 M	4	4
	UNIT-V			
Q.9.	Explain the following with neat sketch. a) Switched capacitor comparator. b) Regenerative comparator.	20 M	5	2
	OR			
Q.10.	Construct the two-stage open-loop comparator and explain its operation.	20 M	5	3

Hall Ticket No: | | | | | | | | | | |

Question Paper Code: 25MBVESTC04

MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(Deemed to be University under Section 3 of UGC Act, 1956)

M.Tech. I Year II Semester (R25) Regular End Semester Examinations - June 2026

EMBEDDED SYSTEM DESIGN

(VLSI Design and Embedded Systems)

Time: 3Hrs **Max Marks: 100**

All parts of a question must be answered in one place only.
Answer one question from each of Units I to V

Q.No.		Question	Marks	CO	BL
		UNIT-I			
Q.1.	a.	Define an Embedded System and explain its characteristics and quality attributes.	20 M	1	2
	b.	Classify embedded systems based on functionality and performance with suitable examples.			
		OR			
Q.2.	a.	Compare Embedded Systems with General Computing Systems.	20 M	1	3
	b.	Analyze the evolution of embedded systems and discuss their impact on modern applications.			
		UNIT-II			
Q.3.	a.	Explain domain-specific and general-purpose processors with examples.	20 M	2	3
	b.	A sensor transmits data at 4800 bps. Calculate the time required to transmit 200 bytes of data.			
		OR			
Q.4.	a.	Compare ROM, RAM, and Flash memory used in embedded systems.	20 M	2	4
	b.	Analyze different communication interfaces (I2C, SPI, UART) used in embedded systems.			
		UNIT-III			
Q.5.	a.	Explain the working of reset circuit, watchdog timer, and real-time clock.	20 M	3	4
	b.	Discuss oscillator units and brown-out protection circuits.			
		OR			
Q.6.	a.	Explain different embedded firmware design approaches.	20 M	3	5
	b.	Design a simple super loop-based firmware for a temperature monitoring system.			
		UNIT-IV			
Q.7.	a.	A smart home system requires multiple sensors and actuators to run concurrently. Analyze the need for RTOS in this system.	20 M	4	4
	b.	Differentiate tasks, processes, and threads with suitable examples.			
		OR			
Q.8.	a.	Explain pre-emptive and non-pre-emptive scheduling techniques.	20 M	4	5
	b.	Four tasks T1 (4 ms), T2 (3 ms), T3 (2 ms), T4 (1 ms) are scheduled using Round Robin (time quantum = 2 ms). Illustrate scheduling.			

UNIT-V

Q.9.	a.	Discuss deadlock conditions and methods to prevent them.	20 M	5	3
	b.	Explain task synchronization techniques using semaphores and mutexes.			

OR

Q.10.	a.	An autonomous vehicle system processes multiple sensor inputs. Recommend suitable inter-task communication techniques.	20 M	5	5
	b.	Demonstrate how shared memory communication can lead to race conditions and how to resolve them.			

*****End*****

Hall Ticket No: | | | | | | | | | | |

Question Paper Code: 25MBVESDC12

MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(Deemed to be University under Section 3 of UGC Act, 1956)

M.Tech. I Year II Semester (R25) Regular End Semester Examinations - June 2026

HIGH SPEED VLSI DESIGN

(VLSI Design and Embedded Systems)

Time: 3Hrs **Max Marks: 100**

All parts of a question must be answered in one place only.
Answer one question from each of Units I to V

Q.No.		Question	Marks	CO	BL
		UNIT-I			
Q.1.		Discuss the impact of technology scaling on VLSI circuit performance.	20	1	3
		OR			
Q.2.		Explain the importance of delay minimization in high-speed VLSI design.	20	1	2
		UNIT-II			
Q.3.		Examine the different interconnect parasitics present in VLSI circuits and discuss their impact on circuit speed and performance.	20	2	2
		OR			
Q.4.		Discuss the major signal integrity issues encountered in high-speed VLSI circuits and explain their impact on reliable circuit operation.	20	2	3
		UNIT-III			
Q.5.	a.	Design and analyze a static CMOS gate for the Boolean function Y=(A+B)(C+D). Discuss the pull-up and pull-down network design, propagation delay, power dissipation, and transistor count.	20	3	3
	b.	Describe any two low-power design techniques used in VLSI with an example for each.			
		OR			
Q.6.		Design a domino logic circuit for Y=(A+B+C) D and explain the operation of the dynamic stage and static inverter. Discuss cascading issues and noise immunity.	20	3	3
		UNIT-IV			
Q.7.		Explain latch-based clocking techniques and discuss their advantages over edge-triggered flip-flop-based systems	20	4	2
		OR			
Q.8.		Discuss clock jitter and its impact on the performance of high-speed digital circuits.	20	4	3
		UNIT-V			
Q.9.		Explain different techniques used to improve the performance of on-chip interconnects. Discuss buffering, repeater insertion, shielding, differential signaling, and low-swing signaling techniques.	20	5	3
		OR			
Q.10.		Analyse current industry trends in high-performance VLSI systems. Discuss the role of AI accelerators, heterogeneous computing, chiplet-based architectures, advanced packaging technologies, and high-bandwidth memory (HBM) in modern system design.	20	5	3

End

Hall Ticket No: | | | | | | | | | | |

Question Paper Code: 25MBVESDC07

MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(Deemed to be University under Section 3 of UGC Act, 1956)

M.Tech. I Year II Semester (R25) Regular End Semester Examinations - June 2026

PATTERN RECOGNITION AND MACHINE LEARNING

(VLSI Design and Embedded Systems)

Time: 3Hrs **Max Marks: 100**

All parts of a question must be answered in one place only.
Answer one question from each of Units I to V

Q.No.	Question	Marks	CO	BL
	UNIT-I			
Q.1.	Outline about the role of Bayesian decision theory in the design of pattern classifiers. Also, describe the concept of the Bayes error rate, and discuss its significance in evaluating the performance of classifiers, particularly in multiclass scenarios.	20 M	1	2
	OR			
Q.2.	Analyze the pattern recognition role in machine learning, providing detailed examples from diverse domains such as image recognition, speech processing, and medical diagnostics.	20 M	1	4
	UNIT-II			
Q.3.	Consider the following data points $y=3x+2$	20 M	2	3

x	1	2	3	4	6
y	5	8	11	14	20

evaluate the polynomial approximation of the data using the least squares method. Based on this model, interpret its accuracy and compute the predicted value f(5).

	OR				
Q.4.	Analyze the linear regression model by deriving its parameter estimation using the least squares method. Interpret the effectiveness of this approach in minimizing error and assess how the model's performance varies when applied to diverse datasets with differing characteristics.	20 M	2	4
	UNIT-III			
Q.5.	Analyze the trade-offs involved in selecting kernel functions for support vector machines and Gaussian processes. How do different kernel choices affect model flexibility, computational efficiency, and the risk of overfitting or underfitting on various datasets.	20 M	3	4
	OR			
Q.6.	Determine the N-W estimator within the framework of radial basis function networks. Provide a detailed analysis of its bias-variance characteristics as a function of kernel width and mathematically relate its operation to non-parametric kernel density estimation.	20 M	3	4
	UNIT-IV			
Q.7.	Outline the use of graphical models in time-series analysis (e.g., hidden Markov models or dynamic Bayesian networks). Discuss the unique challenges posed by temporal dependencies.	20 M	4	2
	OR			

Q.8.	Distinguish between the inference on chains, trees, and general graphs and also discuss the computational complexity and exactness of inference in each case.	20 M	4	4

UNIT-V

Q.9.	Explain the use of EM in mixtures of expert's models. How does the gating network interact with the expert components, and what are the implications for interpretability and overfitting?	20 M	5	2

OR

Q.10.	Summarize about the limitations of K-means clustering for image segmentation and explain how Gaussian Mixture Models (GMMs) overcome these limitations. Illustrate your answer with practical examples.	20 M	5	2

*****End*****